STATUS OF THE CLAIMS

The status of the claims of the present application stands as follows:

1. **(Original)** A method of placing a first integrated circuit macro in a floor plan containing at least one second integrated circuit macro, comprising the steps of:
   a) defining edge constraints on at least one edge of the first integrated circuit macro;
   b) defining edge constraints on at least one edge of the second integrated circuit macro; and
   c) automatically comparing said edge constraints on said at least one edge of the first integrated circuit macro and said edge constraints on said at least one edge of the second integrated circuit macro with one another.

2. **(Original)** A method according to claim 1, wherein step c) includes performing a string searching algorithm.

3. **(Original)** A method according to claim 1, further comprising the steps of generating a first edge constraint vector corresponding to said at least one edge of the first integrated circuit macro and generating a second edge constraint vector corresponding to said at least one edge of the second integrated circuit macro.

4. **(Original)** A method according to claim 3, further comprising the step of assigning signatures to said edge constraints of corresponding respective ones of said at least one edge of the first integrated circuit macro and at least one edge of the second integrated circuit macro.

5. **(Original)** A method according to claim 1, further comprising, prior to step a), the step of defining a common unit of measure for use in steps a) and b).

6. **(Original)** A method according to claim 5, wherein each of steps a) and b) includes measuring each of said edge constraints using said common unit of measure.

7. **(Original)** A method according to claim 6, wherein each of steps a) and b) further includes assigning a signature to each unit of measure located within each of said edge constraints.

8. **(Original)** A computer readable medium containing computer executable instructions implementing a method of placing a first integrated circuit macro in a floor plan containing at least one second integrated circuit macro, the instructions comprising:
   a) a first set of instructions for defining edge constraints on at least one edge of the first integrated circuit macro and defining edge constraints on at least one edge of the second integrated circuit macro; and
   b) a second set of instructions for comparing said edge constraints on said at least one edge of the first integrated circuit macro and said edge constraints on said at least one edge of the second integrated circuit macro with one another.

9. **(Original)** A computer readable medium according to claim 8, wherein said second set of instructions includes instructions for performing a string searching algorithm.

10. **(Original)** A computer readable medium according to claim 8, further comprising instructions for generating a first edge constraint vector corresponding to said at least one edge of the first integrated circuit macro and generating a second edge constraint vector corresponding to said at least one edge of the second integrated circuit macro.

11. **(Original)** A computer readable medium according to claim 10, further comprising instructions for assigning signatures to said edge constraints of corresponding respective ones of said at least one edge of the first integrated circuit macro and at least one edge of the second integrated circuit macro.

12. **(Original)** A computer readable medium according to claim 11, further comprising instructions for measuring each of said edge constraints using a common unit of measure.

13. **(Original)** A computer readable medium according to claim 12, further comprising instructions for assigning a signature to each unit of measure located within each of said edge constraints.

14. **(Original)** A CAD system, comprising:
   a) a GUI interface having a floor plan region and operatively configured to allow a user to place a plurality of integrated circuit macros in said floor plan region, each of said

integrated circuit macros having a plurality of edges each having one or more edge constraints; and

b) an integrated circuit macro placing module operatively configured to compare said one or more edge constraints of a first integrated circuit macro to said one or more edge constraints of a second integrated circuit macro.

15. **(Original)** A system according to claim 14, wherein said integrated circuit macro placing module is operatively configured to compare said one or more edge constraints of a first integrated circuit macro to said one or more edge constraints of a second integrated circuit macro using a string matching algorithm.

16. **(Original)** A system according to claim 14, wherein said integrated circuit placing module comprises an edge constraint defining sub-module operatively configured to generate an edge constraint definition for each of said plurality of edges of said plurality of integrated circuit macros.

17. **(Original)** A system according to claim 14, wherein said integrated circuit placing module comprises placing sub-module operatively configured to determine, when at least one of said plurality of macros has been placed in said floor plan region, whether any of said plurality of edges of said at least one of said plurality of macros present in said floor plan region are active edges.

18. **(Original)** A system according to claim 17, wherein said integrated circuit placing module comprises an edge constraint vectorizing sub-module operatively configured to generate an edge constraint vector for each of said active edges when at least one of said plurality of macros has been placed in said floor plan region.

19. **(Original)** A system according to claim 17, wherein, when at least one of said plurality of integrated circuit macros has been placed in said floor plan region, said GUI interface is operatively configured to highlight said active edges.

20. **(Original)** A system according to claim 14, further comprising CAD software.